REMARKS

The Office Action of **August 21, 2001** has been received and its contents carefully noted. Filed concurrently herewith is a *Request for a One (1) Month Extension of Time* that extends the shortened statutory period for response to **December 21, 2001**. Accordingly, Applicants respectfully submit that this response is timely filed and fully responsive to the Office Action.

Claims 12-19, 21-24, 26-43, 46-61 and 65-84 were pending in the present application prior to the aforementioned amendment. By the above Amendment, claims 14, 59 and 72-74 are canceled without prejudice, and claims 12, 18, 23, 29, 34, 37, 41, 53, 55 and 58 are amended to better encompass the full scope and breadth of the invention. Notwithstanding this action, Applicants believe that the claims would have been allowable as originally filed and assert that no issue of new matter is presented and the claims are not narrowing within the meaning of *Festo*. Accordingly, claims 12, 13, 15-19, 21-24, 26-43, 46-58, 60, 61, 65-71 and 75-84 are currently pending in the subject application, and, for at least the reasons advanced below, are believed to be in condition for allowance.

The Office Action rejects claims 12-15, 17, 23-24, 26, 28-31, 33-39, 41-43, 46, 48-61, 65, 67-75 and 77-84 under 35 USC §103(a) as unpatentable over ***Chang '775*** in view of ***Wolf et al.*** and ***Yamazaki et al.*** (U.S. Patent No. 4,727,044), and claims 16, 18-19, 21-22, 27, 32, 40, 47, 66 and 76 under 35 USC §103(a) as unpatentable over ***Chang '775*** in view of ***Wolf et al.***, ***Han et al. '118*** and ***Yamazaki et al. '044***.

By the above actions, claims 14, 59 and 72-74 are canceled without prejudice, thereby rendering the rejection moot with respect thereto. This fact notwithstanding, the rejections with respect to the remaining claims are respectfully traversed for the following reasons. Withdrawal of the rejection and favorable consideration of the

amendments is kindly solicited in view thereof. Applicants hereby incorporate by reference the arguments previously solicited during prosecution of the subject application.

The claimed invention is directed generally to a method for fabricating a semiconductor device comprising the steps of forming a semiconductor film on an insulating surface, forming an insulating film on the semiconductor film, introducing an impurity such as boron into at least a portion of the semiconductor film and through the insulating film, crystallizing the semiconductor film by laser irradiation, removing the insulating film by wet etching, and forming a gate insulating film on the semiconductor film.

As the Examiner well knows, three criteria must be met in order to establish a *prima facie* case of obviousness. *M.P.E.P.* §2143. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings to achieve the claimed invention. *Id.* Second, there must be a reasonable expectation of success. *In re Rhinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976). Third, the prior art must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Applicants respectfully submit that the findings set forth in the Office Action fail to support a *prima facie* case of obviousness under §103, and the claimed invention is patentably distinct over the related art of record. More particularly, Applicants contend that the combined teachings of the proposed ***Chang*** modifications fail to expressly teach or implicitly suggest every claim limitation of the claimed invention. For instance, neither of the proposed ***Chang*** modifications teaches a step of introducing an impurity such as boron into at least a portion of said semiconductor film through an insulating

film, as set forth at least in independent claims 12, 18, 23, 29, 34, 37, 41, 53, 55 and 55 of the claimed invention. Applicants would also like to note that in review of the Office Action, the Examiner failed to specifically address where such a limitation is taught in the proposed ***Chang*** modifications. In this regard, Applicants respectfully request in the next communication that the Examiner specifically address where in either of ***Chang '775***, ***Wolf et al.***, ***Yamazaki et al. '044*** or ***Han et al. '118*** that an introduction of an impurity such as boron into at least a portion of a semiconductor film through an insulating film is proposed.

In Applicants review of the related art of record, it should be further noted that although ***Chang '775*** appears to disclose the formation of a semiconductor layer 34 on an insulating surface 32, ***Chang '775*** expressly discloses at least on column 3, lines 19-22 and column 4, lines 17-26 that boron 36 is introduced into the semiconductor layer 34. Consequently, ***Chang '775*** fails to expressly teach or implicitly suggest introducing an impurity such as boron through an insulating film. This contention is supported by the fact that ***Chang '775*** expressly teaches at column 3, lines 40-50 that an insulating layer 40 is formed subsequent to the step of introducing boron.

On the other hand, practice of the method in accordance with the claimed invention requires formation of the insulating film prior to the step of introducing boron. Accordingly, the presently claimed invention would not have resulted even if one of ordinary skill in the art combines the respective teachings of ***Chang '775***, ***Wolf et al.***, ***Yamazaki et al. '044*** and ***Han et al. '118***.

Applicants submit that the step involving introduction of boron as a p-type impurity is non obviously advantageous over the related art of record since it results in a PTFT having an active layer that exhibits small field mobility. In particular, the PTFT of the claimed invention has a high ON resistance while the OFF resistance is still

sufficiently higher than the ON resistance. Accordingly, an additional capacitance that was conventionally necessary is no longer required. Specifically, the source of a leak current in N-channel MOS, i.e., mobile ions as sodium, pose no threat in the PTFT in accordance with the claimed invention.

In addition, the resultant structure of the semiconductor device that is achieved by practice of the claimed invention cannot be obtained in an N-channel MOS because N-channel MOS's have are characterized by having excessively large leak current due to the presence of fixed charges in the gate oxide film. Although the presence of fixed charges effects the threshold voltage in PTFTs, the leak current in the claimed invention is suppressed to a level such that the essential characteristics for active matrix operation is achieved.

Accordingly, since each of the proposed ***Chang '755*** modifications fail to expressly teach or implicitly suggest a step of introducing an impurity such as boron into at least a portion of the semiconductor film and through the insulating film, the advantageous results produced by the claimed invention cannot be achieved.

In accordance with the claimed invention, Applicants further submit that the step of removing the insulating film from the semiconductor film by a wet etching process is non obviously advantageous over conventional dry etching processes. In contrast to dry etching processes, which damage the silicon film, the step of removing the insulating film from the semiconductor film by wet etching results in a semiconductor device having enhanced electrical characteristics. In particular, Applicants have found that wet etching provides an extremely stable surface by terminating dangling bonds with fluorine and hydrogen before double bonds are formed among the silicon atoms. Applicants respectfully contend that because the combined teachings set forth in ***Chang '775***, ***Wolf***

et al., ***Yamazaki et al. '044*** and ***Han et al. '118*** each fail to expressly teach or implicitly suggest such a feature, the advantageous results produced therefrom cannot be obtained.

Accordingly, since the proposed ***Chang '755*** modifications fail to teach or suggest all the claim limitations, and also fails to teach or suggest the unobvious advantageous properties resulting therefrom, Applicants respectfully request that the claimed invention is patentably distinct over the prior art. Reconsideration and withdrawal is respectfully requested. If the Examiner believes further discussions with Applicants' representative would be beneficial in this case, he is invited to contact the undersigned.

Respectfully submitted,

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Marked-copy of amended claims.

12. (Amended) A method for fabricating a semiconductor device, comprising the steps of:

forming a semiconductor film comprising amorphous silicon on an insulating surface;

forming an insulating film on said semiconductor film;

introducing boron into at least a portion of said semiconductor film though said insulating film, said portion to become at least a channel region;

crystallizing said semiconductor film by laser irradiation through said insulating film;

removing said insulating film by wet etching;

forming a gate insulating film on said semiconductor film;

forming a gate electrode on said gate insulating film, said gate electrode having tapered side edges; and

forming source and drain regions in said semiconductor film by ion doping through said gate insulating film.

18. (Amended) A method for fabricating a semiconductor device, comprising the steps of:

forming a semiconductor film comprising amorphous silicon on an insulating surface;

forming an insulating film on said semiconductor film;

introducing boron into at least a portion of said semiconductor film through said insulating film, said portion to become at least a channel region;

crystallizing said semiconductor film by laser irradiation through said

insulating film;

removing said insulating film by wet etching;

forming a gate insulating film on said semiconductor film;

forming a gate electrode on said gate insulating film, said gate electrode having tapered side edges; and

forming source and drain regions in said semiconductor film by ion doping.

23. (Amended) A method for fabricating a semiconductor device, comprising the steps of:

forming a semiconductor film comprising amorphous silicon on an insulating surface;

forming an insulating film on said semiconductor film;

introducing boron into at least a portion of said semiconductor film though said insulating film, said portion to become at least a channel region;

crystallizing said semiconductor film by laser irradiation through said insulating film;

removing said insulating film by wet etching;

forming a gate insulating film on said semiconductor film;

forming a gate electrode comprising aluminum on said gate insulating film; and

forming source and drain regions in said semiconductor film by ion doping which is performed through said gate insulating film.

29. (Amended) A method for fabricating a thin film transistor of a pixel portion in a semiconductor device, comprising the steps of:

forming a semiconductor film comprising amorphous silicon on an insulating

surface;

forming an insulating film on said semiconductor film;

introducing boron into at least a portion of said semiconductor film through said insulating film, said portion to become at least a channel region;

crystallizing said semiconductor film by laser irradiation through said insulating film;

removing said insulating film by wet etching;

forming a gate insulating film on said semiconductor film;

forming a gate electrode on said gate insulating film; and

forming source and drain regions in said semiconductor film by ion doping.

34. (Amended) A method for fabricating a thin film transistor of a pixel portion in a semiconductor device, comprising the steps of:

forming a semiconductor film on an insulating surface;

forming an insulating film on said semiconductor film;

introducing boron into at least a portion of said semiconductor film through said insulating film, said portion to become at least a channel region;

crystallizing said semiconductor film by laser irradiation through said insulating film;

removing said insulating film by wet etching;

forming a gate insulating film on said semiconductor film;

forming a gate electrode on said gate insulating film; and

forming source and drain regions in said semiconductor film by ion doping.

37. (Amended) A method for fabricating a semiconductor device,

comprising the steps of:

forming a semiconductor film on an insulating surface;

forming an insulating film on said semiconductor film;

introducing boron into at least a portion of said semiconductor film through said insulating film, said portion to become at least a channel region;

crystallizing said semiconductor film by laser irradiation through said insulating film;

removing said insulating film by wet etching;

forming a gate insulating film on said semiconductor film;

forming a gate electrode on said gate insulating film, said gate electrode having tapered side edges; and

forming source and drain regions in said semiconductor film by ion doping.

41. (Amended) A method for fabricating a semiconductor device, comprising the steps of:

forming a semiconductor film on an insulating surface;

forming an insulating film on said semiconductor film;

introducing boron into at least a portion of said semiconductor film through said insulating film, said portion to become at least a channel region;

crystallizing said semiconductor film by laser irradiation through said insulating film;

removing said insulating film by wet etching;

forming a gate insulating film on said semiconductor film;

forming a gate electrode comprising aluminum on said gate insulating film;

forming source and drain regions in said semiconductor film by ion doping

through said gate insulating film.

53. (Amended) A method for fabricating a thin film transistor of a pixel portion in a semiconductor device, said semiconductor device having at least one thin film transistor comprising a semiconductor film formed adjacent to a gate electrode with a gate insulating film therebetween, said method comprising the steps of:

forming said semiconductor film over a substrate;

forming an insulating film on said semiconductor film;

introducing boron into at least a portion of said semiconductor film through said insulating film, said portion becoming at least a channel region of said thin film transistor;

crystallizing said semiconductor film by laser irradiation through said insulating film; [and]

removing said insulating film; and

introducing boron into said semiconductor film to form a source region and a drain region,

wherein said gate insulating film is formed using TEOS.

55. (Amended) A method for fabricating a thin film transistor of a pixel portion in a semiconductor device, said semiconductor device having at least one thin film transistor comprising a semiconductor film formed adjacent to a gate electrode with a gate insulating film therebetween, said method comprising the steps of:

forming said semiconductor film over a substrate;

forming an insulating film on said semiconductor film;

introducing boron into at least a portion of said semiconductor film through

said insulating film, said portion becoming at least a channel region of said thin film transistor;

crystallizing said semiconductor film by laser irradiation through said insulating film;

removing said insulating film; [and]

forming source and drain regions in said semiconductor film by ion doping; and

introducing boron into said semiconductor film to form a source region and a drain region,

wherein said gate insulating film is formed using TEOS.

58. (Amended) A method for fabricating in a thin film transistor of a pixel portion in a semiconductor device, said semiconductor device having at least one thin film transistor comprising a crystalline semiconductor film formed adjacent to a gate electrode with a gate insulating film therebetween, said method comprising the steps of:

forming a semiconductor film comprising amorphous silicon over a substrate;

forming an insulating film on said semiconductor film;

introducing boron into at least a portion of said semiconductor film through said insulating film, said portion becoming at least a channel region of said thin film transistor;

crystallizing said semiconductor film by laser irradiation through said insulating film;

removing said insulating film; [and]

forming source and drain regions in the crystalline semiconductor film by ion doping; and

introducing boron into said semiconductor film to form a source region and a

drain region,

wherein said gate insulating film is formed using TEOS.